WS-120M 2.4GHz RS232 Wireless Adaptor

AirRunner™ Wireless Series

The Zcomax Airrunner WS-120M allows connection of a serial device to a wireless LAN, bringing the convenience and adaptability of wireless networking to serial equipment.

The WS-120M features an Atheros AR6000 series, Radio-on-Chip for Mobile, chipset. This family of chipsets was specifically designed for the requirements of today's mobile devices such as low power consumption, small form factor and low-overhead operation for the host device. Those features, added to the robust performance inherent to Atheros products, the WS-120M promises to bring exceptional performance to the serial market.

Other important features of this unit are a Hirose U.FL antenna connection for fast and reliable deployment and flexibility in antenna options as well as FCC and RoHS compliance.

We are please to offer this product to an important sector of the wireless networking market. For more details such as availability, samples and pricing in regards to the WS-120M or any other Zcomax wireless product, please contact a sales representative today.

Wireless Serial Module

Key Features

- **802.11g compliant**
- **15 dBm Tx output Power**
- **-82 dBm Rx Sensitivity**
- **External Antenna Connection (U.FL)**
- **Serial to WLAN bridge**
- **FCC and ROHS compliant**
- **MAC / Baseband – Atheros**
- **WPA encryption security**

Driver support – Linux customized drivers are available.

WS-120M at a Glance

Chipset	Atheros AR6101VG ROCm
Transmit Power	15 dBm @ 6 ~ 24 Mbps data rate
Receive Sensitivity	-82 dBm @ 11 Mbps data rate
Antenna Connector	1 - U.FL Antenna Connection

IEEE	Radio	RoHS	Interface
IEEE 802.11G	Atheros Communications	RoHS	Serial

Radio Specification				
Standard	IEEE 802.11b/g			
Modulation	OFDM (BPSK, QPSK, 16-QAM, 64-QAM), DSSS (DBPSK, DQPSK, CCK)			
Channel Bandwidth	20 MHz			
RF Frequency	**USA (FCC)**		**Europe (ETSI)**	**Japan (TELEC)**
802.11g	2.412GHz ~ 2.462GHz		2.412GHz ~ 2.472GHz	2.412GHz ~ 2.472GHz
802.11b	2.412GHz ~ 2.462GHz		2.412GHz ~ 2.472GHz	2.412GHz ~ 2.484GHz
RF Output Power (± 1.5dBm)	**Data Rate**	**802.11b**	**Data Rate**	**802..11g**
	1Mbps	15dBm	6 ~ 24MBps	15dBm
	2Mbps	15dBm	36Mbps	14dBm
	5.5Mbps	15dBm	48Mbps	13dBm
	11Mbps	15dBm	54Mbps	11dBm
Receiver Sensitivity	**802.11b**		**802.11g**	
	≤ -82dBm @ 11Mbps (≤ 10% PER)		≤ -72dBm @ 54Mbps (≤ 8% PER)	
Antenna Connection	1 Hirose U.FL Connection			

Physical Specification		
Dimensions	42mm(L) X 36mm(W) X 6mm(H)	
Host Interface	40-pin Link Star P5L21-220D1BKC001 Female Connector	
Working Temperature	-25°C to +70°C, 90% relative humidity (non-condensing)	
Power Requirement	DC 3.3V ± 5%	
Power Consumption	**802.11b**	**802.11g**
	Tx: ≤ 350mA	Tx: ≤ 350mA
	Rx:≤ 250mA	Rx:≤ 250mA

Warranty	
Warranty Period	1 Year limited warranty from the date of purchase
Warranty Plan	Zcomax Repair / Replacement Program

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Zcomax New Jersey
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WS-120M Pin Definition of J1 (P5L21-220D1BKC001) and LGA(AR6101GL)
JP1 (2345-20TD1T)

J1 Pin #	JP1 Pin #	LGA Pin#	Pin Name	Type	Symbol	Description
1,2	—	A2,A3, A4,A12, B3,B4,B1 2,C4,C5, C13,D3, E3,H2	DVDD3	Power	—	Power supply from host
3	13	V11	RTS0- / RTS0	I	GPIO13	(optional) UART Request to Send
4	11	F18	TXD0-/ TXD0	O	GPIO2	UART receive and transmit data, compatible to 16550
5	14	F17	RXD0/RX D0-	I/OL	GPIO3	
6	3	G18	GPIO5	I/OL	GPIO5	General purpose I/O [3-0]. Default to inputs, control using the GPIOCR register. Input from the GPIOs can be read using the GPIODI register. Output to the GPIOs is provided by the GPIODO register.
7	8	G17	GPIO6	I/OL	GPIO6	
9	17	H18	GPIO7	I/OL	GPIO7	
40	—	D18	SPI_CLK	I/OL	GPIO0	
8	10	N18	CTS0-/ CTS0	I	GPIO12	(optional) UART Clear to Send
10	4	H17	GPIO8	I/OL	GPIO8	In SPI mode, an out-of-band wake up signalling on GPIO8 is used to indicate the state the AR6101VG to the host. Once wake-up is initiated, the host waits for an interrupt. An 8 ms timer is used to insure the AR6101VG does not go back to sleep. The host needs to handle the interrupt during this 8 ms.
14	6	U4	GPIO9	I/OL	GPIO9	
18	—	B18	GPIO10	I/OL	GPIO10	
19	—	C18	GPIO11	I/OL	GPIO11	
35	5	N17	GPIO16	I/OL	GPIO16	
36	—	R18	ADC_nCS	—	GPIO15	
37	16	N16	GPIO17	I/OL	GPIO17	
39	7	U11	LCD_nC/D	I/OL	GPIO14	
11,12,2 3,24	19,20	A18, B17, C16, G11, G12, H11, H12, J3, J11, J12,	DGND	Ground	—	Ground
13	—	U3	nSYSRST	I/O	CLK_REQ	When an external high frequency (e.g., 40 MHz) clock source is used, this pin is asserted to notify the host to enable the external clock source. This must be done within 2 ms after CLK_REQ assertion. On de-assertion, the host may disable the external clock to save power. CLK_REQ is a boot configuration pin and is latched upon SYS_RST_L de-assertion. External pull-up needed, must be set high.
15,16	1,2	—	VBATT	Power	—	Power supply from host
17	—	N2	nRSOUT	OH	RST_OUT_L	The AR6101VG asserts this pin when its core is in reset. Must be tied to RESET_L.
20,21,2 2,	9,12,15,1 8	NC	NC	NC	NC	NC
25	—	U13	COL0-/ COL0	—	RES	Reserved, Internal pull-down. Can be left open or connected to ground
26	—	U14	COL1-/ COL1			
27	—	V14	COL2-/ COL2			
28	—	U16	COL3-/ COL3			
29	—	U15	COL4-/ COL4			
30	—	V15	ROW0-/ ROW0			
31	—	V17	ROW1-/ ROW1			
32	—	T17	ROW2-/ ROW2			
33	—	U18	ROW3-/ ROW3			
34	—	F16	TEST_WDT/ CLR_WDT			
38	—	E18	SPI_MISO	I/OL	GPIO1	General purpose I/O [3-0]. Default to inputs, control using the GPIOCR register. Input from the GPIOs can be read using the GPIODI register. Output to the GPIOs is provided by the GPIODO register.

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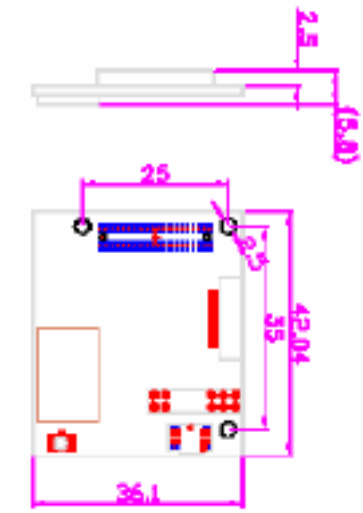
Outline Drawing



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